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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant: Jaroslav Hynecek Docket Number: TI-36483

Serial No.: 10/633,993 Art Unit: 3663

Filed: 08/04/03 Examiner: Johannes P. Mondt

For: Clocked Barrier Virtual Phase Charge Coupled Device Image Sensor

CERTIFICATION OF FACSIMILE TRANSMISSION

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Karen Vertz

2-20-06
Date

FACSIMILE COVER SHEET

X	FACSIMILE COVER SHEET	____	AMENDMENT ___(# pages)___
____	NEW APPLICATION	____	EOT _____
____	DECLARATION	____	NOTICE OF APPEAL
____	ASSIGNMENT	X	APPEAL BRIEF & TRANSMITTAL (13 Pages)
____	FORMAL DRAWINGS	____	ISSUE FEE & PUBLICATION FEE (1 Page)
____	INFORMAL DRAWINGS	____	REPLY BRIEF (IN TRIPLICATE) (# Pages)
____	CONTINUATION APP'N		
____	DIVISIONAL APP'N		

NAME OF INVENTOR(S): Jaroslav Hynecek	RECEIPT DATE & SERIAL NO.: Serial No.: 10/633,993 Filing Date: 08/04/03
TITLE OF INVENTION: Clocked Barrier Virtual Phase Charge Coupled Device Image Sensor	
TI FILE NO.: TI-36483 / DEPOSIT ACCT. NO.: 20-0668	
FAXED: 2-20-06 DUE: 2-20-06 ATTY/SEC'Y: AKS/kjv	

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jaroslav Hynecek **Art Unit: 3663**

Serial No.: 10/633,993 **Examiner: Johannes P. Mondt**

Filed: 08/04/03 **Docket: TI-36483**

For: CLOCKED BARRIER VIRTUAL PHASE CHARGE COUPLED DEVICE IMAGE SENSOR

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Karen Vertz 2-20-06
Karen Vertz Date

Transmitted herewith is an Appeal Brief in the above-identified application. The Commissioner is hereby authorized to charge the ***$500.00*** fee for this appeal, or credit any overpayment to Account No. 20-0668.

Respectfully submitted,

Alan K. Stewart
Registration No. 35,373

Texas Instruments, Incorporated
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Patent Department
Dallas, Texas 75265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jaroslav Hynecek
Art Unit: 3663

Serial No.: 10/633,993
Examiner: Johannes P. Mondt

Filed: 08/04/03
Docket: TI-36483

For: CLOCKED BARRIER VIRTUAL PHASE CHARGE COUPLED DEVICE IMAGE SENSOR

APPELLANTS' BRIEF UNDER 37 C.F.R. §1.192

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Karen Vertz 2-20-06
Karen Vertz Date

Dear Commissioner:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed September 20, 2005. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

02/22/2006 MBINAS 00000035 200668 10633993
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REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

Claims 11-17 are the subject of this appeal. Claims 11-17 are rejected. Claims 1-10 and 18-20 have been withdrawn. This application was filed on August 4, 2003.

STATUS OF THE AMENDMENTS

The Appellants filed an amendment under 37 C.F.R. § 1.111 on May 11, 2005 in response to the Office Action dated February 14, 2005. The Appellants filed an amendment under 37 C.F.R. § 1.116 on November 18, 2005 in response to the Office Action dated September 20, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 10, line 16 to page 14, line 2, provides a concise explanation of the invention defined in independent claim 1. Generation of unwanted clock induced dark current is eliminated in the sensor serial and charge multiplying register pixels by incorporating new CCD register design, whose simplified cross section is shown in drawing 300 in FIG. 3. P-type doped silicon substrate 301 has n-type doped buried layer 302 near its surface. Oxide layer 304 on top of the silicon surface separates substrate 301 from poly-silicon gates 305, 307, and 309. The first deposited layer of poly-silicon forms field plate gates 305, which are connected using metal wiring 306 to bias terminal. The second poly-silicon layer, separated form the first one by an oxide dielectric layer, forms separate and independently biased gate electrodes 307 and 309, which are also connected using respective metal wirings 308 and 310 to corresponding bias terminals. Directionality of charge transfer is established by placing suitable barrier implants 303 under a portion of each gate 307 and 309. There are other possibilities and other implant combinations that can create the desired potential profile within each pixel, which are well known to those skilled in the art, and therefore do need to be described here in any further detail. The above described gate structure, after partial depletion of mobile charge, creates potential profile in each pixel that is described by segments 314, 315, 311, 312, and 313. In this example gate 307 is biased in its high biasing level and gate 309 in its low biasing level. Circles 317 indicate the electron charge transfer within the pixel. It is important to note that field plate gate 305 is biased at a DC biasing level and is not clocked. Introducing field plate into the gate structure

has two advantages. The field plate is used to create a suitable potential profile that confines charge in the direction perpendicular to the plane of the drawing without the necessity for heavily doped p+ channel stops. This eliminates the source of unwanted clocking induced dark current caused by impact ionization within such channel stops. The second advantage is a better control of potential profile when this pixel structure is used in charge multiplying registers and the charge-multiplying gate needs to be biased to high biasing levels necessary for the onset of electron multiplication.

For a better understanding of design details of the serial register of present invention, simplified drawing 400 of an example of one possible layout embodiment is shown in FIG. 4. Drawing 400 also shows the details of the interface region between the CCD memory area and serial register. The memory area consists of CCD columns separated by p+ doped channel stops 401. For simplicity only a conventional VP CCD gate structure 403 is shown with barrier region 405 and well region 404. However, the new CB VP CCD structure, shown in drawing 200, can easily be substituted here as is clear to all those skilled in the art. Gate 403 interfaces with virtual well region 402 and virtual barrier region 406 that further interfaces with field plate region 407 of the serial register. Field plate region 407, formed from the fist poly-silicon layer, has openings 415 and notches 413 that are overlaid by the second poly-silicon layer, which forms gates 409 and 410. Metal wirings 408, 411, and 412 serve as interconnects between gates, the field plate, and the biasing terminals. Charge flow directionality is established by implanting barrier regions 414 and 416 under gates 409 and 410. Charge that is transferred from memory area into the serial register flows from Virtual Barrier region

406 under field plate region 422 and further under gate 409. Charge is confined to stay in these regions by suitable potential barrier forming implants 417 and 418 that have replaced the traditional p+ channel stops used in conventional designs. It is thus apparent that gates 409 and 410, which transport charge in serial register do not overlap any p+ channel stop anywhere. This eliminates generation of spurious clocking induced dark current even for high biases required for the onset of charge multiplication. An important feature introduced in this design is the serial register blooming protection. This is accomplished by incorporating anti-blooming barrier implants 421 under gates 409. When a large amount of charge accumulates under these gates, either from excessive charge multiplication in charge multiplying sections of the register or from summing of several lines of data transferred from the memory into the register, excess charge can harmlessly overflow into drain 419 without corrupting charge signal under neighboring gates 410. Overflow charge collecting drain 419 is connected to biasing terminal by wiring 420. The drain interfaces with active device border 423. It is also apparent to those skilled in the art that it is possible to eliminate drain 419 and replace it with another complete serial register structure described above and transfer overflow charge through another charge confining region, similar to region 422, to this register. Several registers can thus be placed next to each other, their gates ganged together in parallel, and overflow charge transferred from one to the next before the final overflow charge is drained out from the structure. This design option is important for constructing devices that can handle high Dynamic Range signals.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 11 stands rejected under 35 U.S.C. § 102 (b) as being anticipated by U.S. Patent No. 5,502,318. Claim 11 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over U.S. Patent No. 5,388,137 in view of U.S. Patent No. 5,760,430.

ARGUMENT

Rejection under 35 U.S.C. § 102 (b) as being anticipated by U.S. Patent No. 5,502,318

Claims 11-17

Claim 11 includes "... a field plate adjacent to and surrounding the first clocked gate, and coupled to a DC bias source ...". U.S. Patent No. 5,502,318 does not show, teach, or suggest the device of claim 11 because U.S. Patent No. 5,502,318 does not disclose the field plate. Regions 40, 42, 44, and 46 in U.S. Patent No. 5,502,318 are bipolar gates, not field plates.

Rejection under 35 U.S.C. § 103 (a) as being unpatentable over U.S. Patent No. 5,388,137 in view of U.S. Patent No. 5,760,430

Claims 11-17

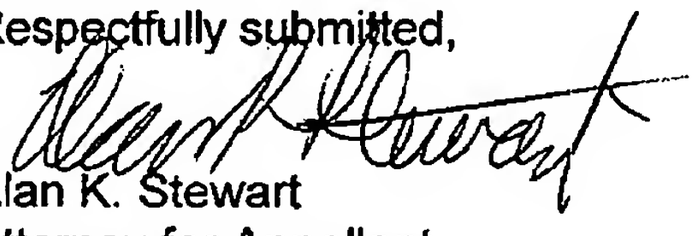
Claim 11 includes "... a field plate adjacent to and surrounding the first clocked gate, and coupled to a DC bias source ...". In U.S. Patent No. 5,388,137, the gate 38 does not surround the first clocked gate 39. The gate 38 is only on one side of clocked gate 39. Gate 40 is on the other side of clocked gate 39. Therefore, in U.S. Patent No. 5,388,137, there is no field plate adjacent to and surrounding the first clocked gate.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 11-17 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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CLAIMS APPENDIX

11. A charge coupled device comprising:

a first clocked gate coupled to a first clocking signal;

a field plate adjacent to and surrounding the first clocked gate, and coupled to a DC bias source; and

a second clocked gate adjacent to and surrounded by the field plate and coupled to a second clocking signal, the field plate separates the first clocked gate from the second clocked gate, and the first clocking signal is clocked out of phase with the second clocking signal.

12. The device of claim 11 wherein the first clocked gate comprises a clocked barrier and a clocked well.

13. The device of claim 12 wherein the second clocked gate comprises a clocked barrier and a clocked well.

14. The device of claim 11 wherein the device is a frame transfer device.

15. The device of claim 11 wherein the device is a full frame device.

16. The device of claim 11 further comprising an antiblooming drain.

17. The device of claim 11 wherein the device is a charge multiplying device.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.